CLAIMS

What is claimed is:

1. A method for testing a device-under-test (DUT), the method comprising the steps of:

examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins; and

separating the first plurality of data units from the second plurality of data units, wherein the first plurality of data units are communicated to the first plurality of DUT pins and the second plurality of data units are communicated to the second plurality of DUT pins.

2. The method of claim 1, wherein the first plurality of data units have at least one different property than the second plurality of data units.

3. The method of claim 2, wherein the at least one different property includes timing complexity.

4. The method of claim 2, wherein the at least one different property includes vector data volume.

5. The method of claim 2, wherein the at least one different property includes repetitive data patterns.

6. The method of claim 1, wherein the first plurality of DUT pins are scan-pins and the second plurality of DUT pins are non-scan pins.

7. The method of claim 1, further comprising the step of:

formatting the first plurality of data units independently from the second plurality of data units.

8. The method of claim 1, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

9. The method of claim 1, wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.

10. A method for testing a device-under-test (DUT), the method comprising the steps of:

examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins; and

identifying the first plurality of DUT pins; and

storing information identifying first plurality of DUT pins in memory.

11. The method of claim 10, further comprising the step of:

providing the information to a module configured to format the test data file.

12. The method of claim 10, further comprising the step of:

formatting the first plurality of data units independently from the second plurality of data units.

13. The method of claim 10, wherein the first plurality of DUT pins are scan-pins and the second plurality of DUT pins are non-scan pins.

14. The method of claim 10, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

15. The method of claim 10, wherein the first plurality of data units have at least one different property than the second plurality of data units.

16. A system for testing a device-under-test (DUT), the system comprising:

memory operative to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins; and

a processor that is programmed to separate the first plurality of data units from the second plurality of data units.

17. The system of claim 16, wherein the processor is programmed to provide the first plurality of data units and the second plurality of data units to a device configured to format the first plurality of data units independently from the second plurality of data units.

18. The system of claim 16, wherein the first plurality of DUT pins are scan-pins and the second plurality of DUT pins are non-scan pins.

19. A system for testing a device-under-test (DUT), the system comprising:

memory operative to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins; and

a processor that is programmed to identify the first plurality of DUT pins based on information contained in the test data file, and to store information identifying the first plurality of DUT pins in memory.

20. The system of claim 19, wherein the processor is programmed to provide the information identifying the first plurality of DUT pins to a device configured to format test data.

21. The system of claim 19, wherein the first plurality of DUT pins are scan-pins and the second plurality of DUT pins are non-scan pins.

22. A system for testing a device-under-test (DUT), the system comprising:

means operative to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins; and

means operative to identify the first plurality of DUT pins based on information contained in the test data file.